Goddard Procedural Requirements (GPR)

DIRECTIVE NO.	GPR 8730.5	**APPROVED BY Signature:**	*Original Signed By*
EFFECTIVE DATE:	March 28, 2016	**NAME:**	Judith N. Bruner
EXPIRATION DATE:	March 28, 2021	**TITLE:**	Director, Safety and Mission Assurance

COMPLIANCE IS MANDATORY

Responsible Office: 300/Safety and Mission Assurance Directorate

Title: Safety and Mission Assurance Acceptance of Inherited and Build-to-Print Products

PREFACE

P.1 PURPOSE

Define an efficient and effective process for dispositioning hardware or software that either already exists or is built-to-print from an existing design based on the risk of using the item in its current form. A prerequisite for deeming such inherited items as acceptable when alternative practices are used is that the items are built using well-established successful processes and requirements for systems developed under a comparable risk posture. This approach enables projects to take credit for inherited or Build-to-Print items having pertinent performance, qualification, operational, manufacturing, and/or reliability history applicable to their mission requirements and provides a means to tailor and/or provide relief to the application of specific Mission Assurance Requirements (MAR) that do not sufficiently contribute to achieving mission success commensurate with their cost baseline and risk posture. This process applies to acquisition of hardware items, including any inherent software used within the item, but not for standalone blocks of software for reuse. If inherited items meet all requirements in the project MAR, then this directive need not be imposed. This directive should be used in lieu of waivers to the MAR for inherited and build-to-print items that are built to alternate requirements.

P.2 APPLICABILITY

This directive applies to all GSFC space flight projects at Greenbelt and Wallops Flight Facility. This directive is optional guidance for other projects, such as suborbital and atmospheric projects.

P.3 AUTHORITIES

NPD 8730.5, NASA Quality Assurance Program Policy
NPD 8720.1, NASA Reliability and Maintainability (R&M) Program Policy

P.4 APPLICABLE DOCUMENTS

NASA-STD-8739.1, Workmanship Standard for Polymeric Applications on Electronic Assemblies

P.5 CANCELLATION

None

P.6 SAFETY

N/A

P.7 TRAINING

None

P.8 RECORDS

Record Title	Record Custodian	Retention
Standard Components Commodity Usage Guidelines (CUG-1)	Reliability and Risk Assessment Branch, Code 371	*NRRS 8/101- PERMANENT. Cut off records at close of program/ project or in 3-year blocks for long term programs/projects. Transfer to national archives 7 years after cutoff.
Software Commodity Usage Guidelines (CUG-2)	Software and Ground Systems Assurance Branch, Code 372	*NRRS 8/101
Digital Electronics Commodity Usage Guidelines (CUG-3)	Reliability and Risk Assessment Branch, Code 371	*NRRS 8/101
Inherited Items Information Package	Project record custodian	NRRS 8/101

** NRRS – NASA Records Retention Schedule (NRRS 1441.1)*

P.9 MEASUREMENT/VERIFICATION

None

PROCEDURES

In this document, a requirement is identified by "shall," a good practice by "should," permission by "may" or "can," expectation by "will," and descriptive material by "is."

1.0 Background

It has become common for significant elements of GSFC spacecraft and instruments to include hardware and software that is either already existing (e.g., a spare board or component from a previous development) or is build-to-print from an existing design. In the realm of these inherited items, it is also common for the items to be built or designed to different SMA specifications than those in the project Mission Assurance Requirements (MAR) document, project system requirements, or in other NASA or GSFC directives. This directive provides a direct means of handling and accepting such items by understanding the previous history (including resolved and unresolved anomalies or failures) of the items, any changes in the item or its on-orbit or testing environment or application, the differences in requirements, and subsequently characterizing and communicating the risk of using the item in its current state. This directive may also be used to aid in accepting commercial-off-the-shelf (COTS) items that are outside of GSFC's experience base. Note that existing hardware may be at any level of assembly, including electrical, electronic, and electromechanical (EEE) parts. For example, this process may be used as an alternative approach to disposition EEE parts that were either pulled from existing stock or procured prior to Parts Control Board approval. Furthermore, this approach may preclude the need for source control drawings or other detailed design deliverables for EEE parts. There is an expectation when using such an alternative approach that the developer has followed some set of established processes and that there is a successful history of similar products under a comparable risk posture. Note that while the information provided may provide a basis for qualification of the items, in general this process should not preclude any elements of environmental test for acceptance, in particular to verify workmanship. The CSO or the Standard Components (SC) Commodity Risk Assessment Engineer (CRAE), in coordination with the Lead Systems Engineer and Project, may reasonably make the determination that the inherited item reviews may be used in lieu of the common component-level milestone reviews Preliminary Design Review (PDR) and Critical Design Review (CDR) for the inherited components.

2.0 Timing

The use of inherited products has multiple insertion points into the life cycle over time and for each point, there are actions that can help ensure an efficient, risk-informed process for incorporating such items into GSFC systems. It is important to consider the attributes of inherited products in the proposal and selection phase, as well as at the point where the products are being delivered. In the earlier phases, GSFC may have less control over how inherited products factor into the overall system, but these phases are included here for those instances where GSFC's interaction can have an impact.

The following represent the top-level guidance applicable to each element, from proposal through development:

Announcements of Opportunity (AOs) and initiation of development partnerships: Define assemblies that are proposed to be inherited or built-to-print inside projects, require vendors to provide sufficient detail, including photographs of inherited hardware. At this point the approach for bringing forth inherited items should be formulated and if the appropriate resources are available, an inherited items planning review should be held with a final product being an agreement on which items should be brought forward as inherited items.

Source Evaluation Boards (SEBs) and Technical Management Cost & Other (TMCO) panels: Provide this document to aid in evaluating list of inherited hardware.

Projects in formulation: Within one month of Mission Concept Review (MCR), vendor, developer, or project office provides the inherited item information in an inherited items information package, as articulated in this document. Representatives from Codes 300, 400, 500, and 600 should participate, Code 800 as applicable. The process may be revisited at any subsequent time when new inherited or Build-to-Print items are added to the design baseline as a result of new requirements, corrective actions to unforeseen design or Integration & Test (I&T) issues, unexpected unavailability of planned hardware, etc.

As early as possible, the SC CRAE should make the determination as to whether the inherited items process is the most effective means of dispositioning the items at hand.

3.0 Information and data required/requested

In order to properly assess the risk of using an inherited item as is, several pieces of information are key to establishing the basis in risk. The vendor/developer should include the following materials as part of the inherited items information package:

a. List of inherited items and statement of approach – rebuild, modification of previous build, or use of existing hardware;
b. Deviations of each item from original design (white wires, cut traces, splices, etc, if not objectively clear to be part of the design) and reasons for each deviation. If the design has been qualified on a previous GSFC project in the same environment and same risk posture, then the deviations may be declared relative to the previously qualified design. See Section 4.5 to consider designs qualified outside of GSFC;
c. Summary results of qualification, acceptance, and/or prototype/protoflight testing completed, or comparison of current qualification/protoqual requirements and what was performed/realized on the inherited design, including environments, required design margins, and life;
d. Flight history of the items and specific attributes for each flight, including environments (compare previous environment to current, including duty cycle and general concept of operations);

e. Ground and on-orbit anomaly and failure history including the determination of root causes or information that root cause was not determined. Ground anomalies may be restricted to major anomalies, where component performance requirements were violated;
f. Specifications and/or standards used to develop the items (e.g., IPC, J-STD, NASA, or GSFC requirements, including fastener integrity approach, or company standards). For items with minimal prior flight history, company standards or detailed synopses of such should be provided, if such are used to develop the product;
g. Previous as-built parts list, including lot date codes, and the differences for new inherited item. This should include evidence that Government Industry Data Exchange Program (GIDEP) alerts and advisories have been properly dispositioned, if the parts have already been procured. Note that GIDEP should always be used as an aid in procuring new parts or pulling parts from inventory. Reference to prior project deliveries to GSFC is acceptable, in which case, an amendment may be delivered to indicate any changes.
h. Known obsolete parts that are intended to be supplied out of existing inventory, along with quantity required vs available in inventory. Sparing plan if available (including quantity required, quantity available, and sparing philosophy).
i. Materials list and approved Material Usage Agreements (MUAs). Materials list includes lot date codes and evidence that GIDEP alerts and advisories have been properly dispositioned, if the materials have already been procured. Such evidence should be encompassed in GIDEP closure records for each of the items that have impacts. Reference to prior project deliveries to GSFC is acceptable, in which case, an amendment may be delivered to indicate any changes.
j. List of major electrical and mechanical analyses completed and summary of results.
k. The reliability analyses performed for the most recent version of the product.
l. Identification of significant changes in manufacturing from qualified unit to current unit (facility, process, subtier supplier, testing changes, company change of ownership, etc)

For items previously used in GSFC projects for which prior complete documentation exists, either in CUG-1 or a comparable record, the vendor/developer may submit documentation that characterizes only the differences between the previous and current application, including the changes in the reliability analyses.

Clearly, it is possible that providing all of the information above may be more challenging than following standard practices for a new development, so the emphasis in compiling this information should be to provide enough to form a clear basis for establishing the risk for using the item without intrusive inspections and requirement verifications internal to the product. The intent is to avoid redesigning a successful design.

The inherited items review should focus on items a, c, d, and e above as these describe the inherited item as a system. These items along with item k should describe the minimum package to determine component-level risk, while the other items focus on risk internal to the item.

4.0 Process elements

The following subsections define the process that culminates in a risk assessment used ultimately to disposition the item. The responsible party for determining the risk associated with use of an inherited item not built to project requirements is the Code 370 Standard Components Commodity Risk Assessment Engineer (SC CRAE). For inherited items likely to be used on multiple projects, the SC CRAE should document the results of the process defined in this directive within the Standard Components Commodity Usage Guidelines (CUG-1).

4.1 Information/data submission

The vendor/developer/project office should provide an initial inherited items information package including, but not necessarily limited to, the listed items in Section 3.0 at Authority to Proceed (ATP) + 30 days, with all updates submitted preferably within a month after MCR, but at least two months prior to Preliminary Design Review (PDR). The SC CRAE shall perform and document an analysis that compares (1) the requirements to produce the item to the project requirements, (2) the environment of previous application in test and on-orbit, to the environments in the current application, and (3) any differences in parts, materials, or construction between the previous and current application

4.2 Inherited Items Review

At least two months prior to the element PDR, the SC CRAE shall chair an Inherited Items Review, including representatives from the project and selected subject matter experts that are independent from the project. The SC CRAE may delegate the chair responsibility as appropriate. The review should cover the list of items in Section 3.0. The formality of the review should be commensurate with the project risk posture.

4.3 Performance assessment vs mission requirements

An assessment should be performed of the item's performance against the mission requirements, to answer the question as to whether the item is suited for the application.

4.4 Workmanship assessment

A qualitative assessment should be performed to determine if the item meets GSFC workmanship requirements commensurate with the risk classification, or amounts to an equivalent level of risk. As with the statement in 3.0, this element is an internal look within the item so a strong basis of successful flight history of the item in the appropriate environment may preclude the need for a detailed workmanship comparison. In most cases after a review of developer practices, workmanship may be verified through environmental testing.

4.5 Prior qualification of inherited item

The vendor/developer/project office may provide evidence that the item in its current form has been fully qualified. On the determination of the SC CRAE, this evidence may fully or partially supersede other requirements and guidance in this document. Note that acceptance of a specific item for flight use is not generally covered through an argument of prior qualification. Acceptance will include elements of workmanship verification, through inspections and/or environmental test. Clearly to fully benefit from this approach, in most cases, workmanship verification and other aspects of acceptance may only be performed through testing on an assembled product. For example, a Field Programmable Gate Array (FPGA) that is an exact duplicate of a previously-flown FPGA may be considered fully qualified by prior flights if the new environment is enveloped by the previous environment and no anomalies have occurred that indicate defects in the design. Minor changes in the design and environment may be addressed by analysis of the differences or the performance of appropriate environmental testing. The digital electronics CRAE should make the determination as to whether analysis is sufficient to assess risk based on the particular design changes.

4.6 Updated reliability analysis

The provider shall ensure that any changes in the configuration, content, environment, or operation of the inherited item are incorporated into the reliability analyses of the previous product. If none of the aforementioned factors have changed, then the prior reliability analyses will suffice as reliability analyses for the current product.

4.7 Software

Special considerations should be given to the acceptance of software as an element of an inherited hardware component. The principles above should be selectively applied. The following guidance should be used specific to the software in an inherited item.

a. Review software requirements and specifications for compatibility with the project;
b. Evaluate previous build documentation for completeness to satisfy an effective Inherited Item Review;
c. Evaluate original development processes;
d. Evaluate failure analyses, on-orbit anomalies, and problem reports for impact to the project;
e. Evaluate fault protection philosophy and assure appropriate analyses identify fault containment rationale and levels of redundancy to meet requirements;
f. Evaluate testing methodologies of previous programs; and
g. Assure that configuration changes are well documented and understood.

Software assurance should make the assessment as to whether the software in the inherited item amounts to reuse, minor modifications to prior software, or re-engineering.

An appropriate representative from software assurance shall then perform a risk assessment, considering:

a. Criticality
b. Redundancy
c. Margins
d. Software impacts on life limited items
e. Statistics that would indicate failure
f. Successful time in test and on-orbit

The SC CRAE or project software quality assurance lead shall ensure that the results of the software inherited item risk assessment are documented in the software Commodity Usage Guidelines (CUG-2) document. Appendix D includes a checklist to aid in dispositioning inherited software.

4.8 Field Programmable Gate Arrays and related technologies

Special considerations should be given to the acceptance of previously flown, altered, or customized field programmable gate arrays (FPGAs), masked programmable gate arrays and other closely related hardware devices. The principles in Sections 1-4 should be selectively applied. The following guidance should be used specific to these types of inherited digital electronic items.

a. Review the original development plan or assurance plan associated with the part in its previous application;

    (1) If no plan exists, then the design and environment should be identical to previously flown versions to make use of this process as an alternative to the requirements in the pertinent project mission assurance requirements document unless the Digital Electronics (DE) Commodity Risk Assessment Engineer (CRAE) determines that the plan is not necessary.

b. Review peer review documentation from the previous application (Peer review information content is in Appendix E)
    (1) Completeness of peer review documentation and level of similarity to previous design should drive the extensiveness of peer review for the current design required
    (2) In some cases, previously flown designs proposed for environments enveloped by prior flight and testing history may not require additional peer review.
c. Review records of failure analyses, on-orbit anomalies, and problem reports for impact to the project, and how they were dispositioned;
d. Evaluate testing methodologies of previous programs;
e. Assure that all configuration aspects, especially any differences, are well documented , such as with a "was/is" table of:

    (1) Full manufacturer part number

(2) Lot/Date code(s)
(3) Vendor part number (e.g., Altered Item Drawing number, etc.)
(4) Logic (e.g., any changes in the hardware description language code, etc.)
(5) Synthesis (e.g., not re-synthesized, re-synthesized to preclude GIDEP xyz, etc.)
(6) Layout (e.g., not re-routed, re-routed per GIDEP xyz, etc.)
(7) Verifications
    (a) Simulations (e.g., not re-run, new simulations added, etc.)
    (b) Analyses (e.g. not updated, timing analysis updated with values exported from latest software version that supports this FPGA, etc.)
    (c) Tests
(8) Environments
    (a) Operating temperature range
    (b) Operating voltage range(s)
    (c) Radiation

f. Assure any differences from the inherited item, such as a newer lot/date code, are agreed as producing an equivalent item
g. Review pertinent GIDEPs released prior to and since the FPGA was developed, including prior disposition reports, for both the FPGA and all software used to develop it

The DE CRAE will make the determination of risk based on the information provided and will make the determination whether minor changes in the design from prior use are substantial enough to warrant a full peer review, a limited scope peer review, or no peer review at all.

The DE CRAE or SC CRAE shall ensure that results of the FPGA inherited item risk assessment are documented in the Digital Electronics Commodity Usage Guidelines (CUG-3) document. Appendix E includes a list to aid in dispositioning inherited FPGAs.

4.9 Application-Specific Integrated Circuits

Special considerations should be given to the acceptance of previously flown, altered, or customized Application-Specific Integrated Circuits (ASICs). The principles in Sections 1-4 should be selectively applied. The following guidance should be used specific to these types of inherited digital electronic items.

a. Review the original development plan or assurance plan associated with the part in its previous application;

    (1) If no plan exists, then the design and environment should be identical to previously flown versions to make use of this process as an alternative to the requirements in the pertinent project mission assurance requirements document unless the Digital Electronics (DE) Commodity

Risk Assessment Engineer (CRAE) determines that the plan is not necessary.

b. Review peer review documentation from the previous application (Peer review information content is in Appendix E)
   (1) Completeness of peer review documentation and level of similarity to previous design should drive the extensiveness of peer review for the current design required
   (2) In some cases, previously flown designs proposed for environments enveloped by prior flight and testing history may not require additional peer review.

c. Review records of failure analyses, on-orbit anomalies, and problem reports for impact to the project, and how they were dispositioned;
d. Evaluate testing methodologies of previous programs;
e. Assure that all configuration aspects, especially any differences, are well documented, such as with a was/is table of:
   (1) Requirement specification
   (2) Block diagram
   (3) Source code (e.g. VHDL or Verilog), PDF of schematics and/or state machines/tables
   (4) Source code for 3rd party intellectual property and/or cores
   (5) Synthesis constraint and report files
   (6) Formal verification (e.g. equivalency checking) results/reports
   (7) Design (place and route) database and constraint file(s)
   (8) Static timing analysis results including best and worst case, and least margin/slack for each
   (9) Timing analyses for external inputs and outputs, internal domain(s), etc.
   (10) Disposition/analysis report of all clock domain crossings
   (11) Verification plan
   (12) Verification test bench/code and final code coverage metrics with list and explanation of any exclusions
   (13) Listing of all bugs detected during verification and their disposition
   (14) Final verification report showing all requirements have been verified (RTL and Back-annotated)
   (15) Design review documentation, presentations, and action item dispositions
   (16) ASIC vendor checklists, including ERC/DRC/LVS results
   (17) Final fault coverage (Was Scan implemented?)
   (18) Listing of any anomalies seen in test or operation in prior projects and their disposition

The following items provide additional useful information to aid in determining risk:

a. System, box, and circuit board requirements, specifications, presentations, and/or verification document(s) relevant to the ASIC and its role in the system, box, and board
b. Board(s) schematics containing this ASIC

c. Board netlist(s) (any American Standard Code for Information Interchange (ASCII) format such as PADS, MGC, Allegro)
d. Board part list (any ASCII or common spreadsheet format)
e. PDF of the board layout, such as an assembly drawing
f. Signal integrity analyses relevant to this ASIC
g. Power integrity analyses relevant to this ASIC. Assure any differences from the inherited item, such as a newer lot/date code, are agreed as producing an equivalent item

The DE CRAE will make the determination of risk based on the information provided and will make the determination whether minor changes in the design from prior use are substantial enough to warrant a full peer review, a limited scope peer review, or no peer review at all.

The DE CRAE or SC CRAE shall ensure that results of the ASIC inherited item risk assessment are documented in the Digital Electronics Commodity Usage Guidelines (CUG-3) document.

4.10 Quality control, in-house vs out-of-house

For commercial products and standard components that are built repeatedly with minimal changes and that have substantial successful flight history, and procured under fixed-price contracts where the developer assumes the risk, quality control should be established by prior history, periodic audit or assessment, and in some cases by minimal key inspections (e.g., mandatory inspection points). In-house NASA builds shall follow pertinent NASA requirements and guidelines; however, for repeat builds of items where subsequent applications are under different risk classifications, changes to guidelines that are based on changes in risk classification should be avoided unless there is evidence of a problem associated with the requirements used for the prior build. A change to any requirements from an existing successful design, even if more stringent, is likely to increase the risk for the new build. Local approaches to quality control and assurance should apply for inherited items.

5.0 Risk Assessment

The SC CRAE shall perform a risk assessment based on the compilation of information and the inherited items review, resulting in a risk statement with a likelihood and consequence in the standard GSFC 5x5 format, or a statement that there is no elevated risk associated with use of the item. The SC CRAE is responsible for leading the risk assessment, with support from other individuals such as the project reliability and risk engineer, the product design lead, and other subject matter experts as needed. Appendix C may be used as an aid to consider the risk implications of common classes of board modifications. The risk determined will be forwarded to and subsequently managed by the project. Note that it is up to the project to make the decision to use as is, or whether mitigations will be performed. The risk may be per item or rolled up collectively over multiple inherited items as reasonable.

Appendix A: Definitions

A.1 Build-to-Print Item: An item that per contract or up-front formal agreement within a project is built to a set of design documentation and drawings. Any changes from the documentation will result in costs outside of the budget for the item.

A.2 DE CRAE: Engineer responsible for tracking, qualifying maintaining lessons learned on, and assessing risk on the use of digital electronic components used on GSFC projects. Note that the DE CRAE may be temporarily appointed by Code 300 if the formal position is vacant.

A.3 Inherited Item: An item brought in to a project as a fully designed item that has some amount of prior history that may be built to different standards than those in project mission assurance requirements, and may not have had NASA insight into the design or construction.

A.4 Risk: The combination of a) the probability (qualitative or quantitative) that an organization will experience an undesired event such as cost overrun, schedule slippage, safety mishap, or failure to achieve a needed technological breakthrough; and b) the consequences, impact, or severity of the undesired event were it to occur.

A.5 SC CRAE: Engineer responsible for tracking, qualifying, maintaining lessons learned on, and assessing risk on the use of standard spacecraft components used on multiple projects.

A.6 Waiver: A specific written authorization granting relief from one or more requirements herein.

Appendix B: Acronyms

AO	Announcements of Opportunity
ASCII	American Standard Code for Information Interchange
ASIC	Application Specific Integrated Circuit
ATP	Authority to Proceed
CDR	Critical Design Review
COTS	Commercial Off The Shelf
CRAE	Commodity Risk Assessment Engineer
CSO	Chief Safety and Mission Assurance Officer
CUG	Commodity Usage Guidelines
DE	Digital Electronics
EEE	Electrical, Electronic, and Electromechanical
FPGA	Field Programmable Gate Array
FRB	Failure Review Board
GIDEP	Government Industry Data Exchange Program
GPR	Goddard Procedural Requirement
GSFC	Goddard Space Flight Center
I&T	Integration & Test
MAR	Mission Assurance Requirements
MUA	Material Usage Agreement
NASA	National Aeronautics and Space Administration
PCB	Printed Circuit Board
PDF	Portable Document Format
PDR	Preliminary Design Review
PG	Procedures and Guidelines
PWA	Printed Wiring Assembly
RTL	Register Transfer Level
SC	Standard Components
SEB	Source Evaluation Board
SMA	Safety and Mission Assurance
TMCO	Technical, Management, Cost, & Other
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuit

Appendix C: Board Modifications

This Appendix provides the information required to both describe the modifications as part of an inherited hardware description package and to use as part of the risk assessment process. The use of the term "white wires" indicates that circuit connections have been rerouted using added jumper wires and cut printed circuit board traces. In these cases, different electronic parts may be swapped into pads for which they were not originally designed, creating additional concerns.

In the past, these types of boards have been evaluated solely on the basis of the quality of the modifications (e.g. solder joints, positioning of the wires, polymeric staking of upside-down packages); that is, on the basis of the Workmanship requirements. There has been less emphasis on the modifications' effect on reliability, i.e., do we feel that this modification may result in early failures or anomalies. The core concern that the project should focus on is "Why are each of the modifications there?" Are there buried problems that have not been fully resolved or has the design changed so much from the original design that its suitability for the current application has been lost? An understanding is needed about what led to the changes and the purpose for each one of the modifications, followed by a risk assessment for the complete product. A respin of the board does not generally mitigate the most significant risk and may further bury the core issues underneath a false sense of security.

In practice, a large quantity of boards will end up with some types of modifications somewhere through the development cycle, and when they occur, generally a failure review board or material review board will have been involved in authorizing the mod, agreeing on the depth of solution to the problem, and capturing any associated risks. The biggest concern for white wires and modifications is on inherited hardware, where NASA has had no part in resolving the problems that led to the changes or the decision to modify a previous design to try to meet current requirements. This Appendix explains this topic and recommends actions that should be taken by Projects and the SMA personnel supporting those Projects, when this situation is encountered. The emphasis should be around what is the risk of using the board and what mitigations can be performed within project resources.

Forward:

In the design and development of an electronic printed wiring assembly (PWA) for a NASA mission, it is almost inevitable that the design of the printed circuit board (PCB) will require corrections or modifications after it has been realized in its manufactured form. This practice is often referred to as adding "White Wires" due to the historic color of the fluoropolymer insulation on the wires that are added to the board for this purpose (current practice has included the use of polyimide-coated wires that appear orange). Another term for a "white wire" is "jumper", although in some circles the jumper wire is considered a wire designed in, while a white wire is a modification to an earlier design. In an ideal world a flight PCB should have no wires added after the board has been designed, reviewed, manufactured, and populated with electronic parts, nor should there be any traces cut from the PCB. This does not preclude the use of wires on a board that are a part of the board from day one (e.g. wires connecting side-entry package leads, which cannot be formed, to the PCB surface). But in order to balance performance with cost and schedule in a low-volume manufacturing environment as applicable to most

NASA missions, mistakes, and new, late-breaking design requirements, are addressed through modifications to the assembled PWAs. Is there a magic number of modifications that a board can tolerate? There really is not, so we steer the question to be, "what is the risk of using the modified board and are there any substantive mitigations that can be performed within the project's resources, without causing undue risk in another area?"

When is a "White Wire" a White Wire?

Looking back in history PCBs were designed with wires, as well as the traces on the board itself. Single layer boards demanded wire connections when one trace had to cross over another trace. Wires connected to a board can be very reliable if the board is designed to have the wire. Turret terminals were often used to terminate a wire to a board. The turret terminal provided a very robust mechanical connection to the board. Some newer boards have gone to a large solder pad to accommodate a wire with solder being used as the mechanical and electrical glue. Solder is not a good structural connection as it is prone to creep-to-rupture failures. The pad needs to be large enough and the wire long enough to lower the stresses internal to the solder and between the pad and the PCB, but in many cases you can only control the pad size if you have space for a glue-on pad. Staking is required on wire lengths of 1 inch or longer to shield the solder joint from tensile stress.

For this Appendix a white wire is a wire that is not part of the original PWA design and it is attached to a pad not originally intended to have a wire attached, or to a pad already occupied by a soldered part lead. Revisions incorporating modifications are revisions and cannot be "reborn" as an original design. Secondary PWAs (Daughter Cards) and piggy-backed parts that are added to cover some form of design problem are also considered part of the "white wiring" problem.

Staking

Staking material, while necessary for mechanical support of a white wire, can also become part of the problem. Staking will expand and contract with thermal cycling and if not placed with insight into its mechanical behavior, can transfer prolonged or cycling stress to the solder joint.m Staking of white wires can involve placing staking on top of other parts; a practice that is not permitted by NASA-STD-8739.1 Polymeric Applications. Piggybacking parts, which normally involves staking, is not allowed by NASA- STD-8739.1 but is often done in a white wire modification. These arrangements create uncharacterized configurations whose design margins and reliability cannot be determined.

Cut traces

PWBs that have cut traces are another reality, but they factor into elevating the risk of using the board. Boards that have been cut to disconnect a trace provide a moisture ingress point. Trapped moisture in PCBs provides the opportunity for layer delamination and metal filament growth between buried trace and barrel conductors. Metal migration of this type is a latent defect. When considering risk involving traces cut, the storage environment should be strongly considered, as well as bakeouts and conformal coat. Some recommended mitigations are: 1) clean cuts of the traces with a minimum gap length, 2)

minimize the disturbance of the underlying board material, 3) clean the area to remove any metallic Foreign Object Debris (FOD), 4) encapsulate the area to eliminate moisture ingress and to hold down the two broken ends of the cut trace.

Reworked solder pads

Solder pads that have had a soldering iron applied more than once are likely to result in elevated risk. Studies dating back to the 1970's show that a single extra soldering thermal cycle can significantly decrease the reliability of internal trace-to-barrel connections in PCBs. Excessive soldering temperatures at pad locations lead to lifted pads. State-of-the-art PCBs are more susceptible to this damage because they have higher layer numbers and require more aggressive heating to reach soldering temperatures. Hand-soldering, such as is done to add individual components and white wires, concentrates this higher heat in a very small, single location, which is a worst-case stress condition for the laminate and metal traces that have very different coefficients of thermal expansion. Some recommended mitigations are: 1) whenever possible, use the most qualified rework operator, 2) use the finest tipped Metcal soldering iron available for SMT pad to white wire work, 3) Use a localized hot air rework approach when viable 4) Perform high magnification (40X) inspection after the rework to ensure that the integrity of the pads or underlying board material has not been compromised.

Good and bad reasons for "White Wires"

There are a variety of reasons for using a wire on a PWA, but in general the reasons fall into the following categories:

1. The need to get power or a signal onto or off of the board. These should be known in advance and designed into a board. Thermocouples are a special case where long leads are common, with the thermocouple on top of a hot part or next to a hot part where traces internal to the board are not practical. (By the definition given above these would not be considered white wires.)

2. Board layout mistakes where the part size or footprint was different from what was expected, resulting in a mismatch between the board pads and the part.

3. Requirements changes that came in after the PCB was laid out. This would include known requirements that were not met and found lacking during testing.

4. Old or new design deficiencies requiring fixes due to errors found in analysis, test, or on-orbit performance of current or previous versions.

5. Mistakes made in manufacture of the bare board where there are missing or extra connectors.

6. Missing traces due to artwork errors.

Problems with White Wires

The addition of white wires may represent an increase in system risk by adding failure points to the PWA. Failure mechanisms introduced by the addition of a white wire include:

1. Broken solder joints
2. No solder in the electrical joints
3. Poor stress relief
4. Thermal stress to the PCB (lifted pads and traces, cracked barrel-to-trace internal connections)
5. Stressed electrical parts (Thermal and Electrical)
6. Poor and incomplete up-front design work that is often compounded by design changes done by designers other than the original designer. Incomplete thinking.
7. Wires that cross over other wires
8. Wires that cross sharp edges
9. Introduction of new single point failures.
10. Introduction of new noise paths.
11. New logic errors
12. Failure due to bullet-proofing (protection circuits with added unintended effects)
13. Wiring errors
14. Timing errors
15. Introduction of sneak circuits or new, undesired grounding paths

White wires as an indication of the thinking that went into the design of the PC Board.

The question asked about a PWA with many white wires on it is, “When does a PC Board have too many cuts and white wires on it, such that it should be disqualified from flight.” There is no obvious answer to this question that involves only counting cuts and “white wires” and the determination should always be made by a detailed risk assessment, where determination of usability is based on the project’s ability to accept or mitigate the risk. An approach to evaluating the implications of cuts and “white wires” must answer a list of questions, including the following:

1) Did the board design include the jumpers from the beginning?

2) Was the design built with wires in mind? (NASA soldering standards consider wires to be components)

3) Are white wires added to cover a small number of mistakes in the footprints?

4) Are the wires a sign of a failed design?

5) Through time has the original designer moved on to new projects, become no longer available or just forgotten the design and its unique behaviors?

If we look back in history we see examples of designs that were all wires; they were designed this way and were shown to be robust in performance and reliability. This case would be addressed by questions 1 and 2 above. The wires referenced in questions 1, and 2 if answered in the affirmative, are not white wires by definition. Questions 3 and 4 require a philosophical answer. With the addition of the first white wire or cut trace the signs of a failed design or deviation from original intended design become evident; the design is no longer whole. As more white wires appear, it becomes clear that either the original design is flawed or that the changes to that design to meet current requirements are so significant that it is no longer practical to assess the current board on the original design.

As white wires are added and cuts are made, the opportunity for installing defects into the assembly is increased as is the opportunity for overlooking those defects during inspections. Past uses of white wires have employed daisy-chained wire sections using crimp connections without the benefit of customized quality criteria. In one case amidst an array of modifications to flight hardware late in I&T, the solder was never applied in two different locations. The lack of solder was missed during the inspection of the joints. The missing solder was missed by 8 different sets of eyes, and it was only after a part failed due to the lack of solder, that the missing solder was discovered. Adding wires also can lead to wires hiding other wires and preventing wires from being inspected. A hidden wire or hidden joint may be non-inspectable for defects even with X-ray systems.

The use of white wires is an indicator that significant risk may exist from a lack of attention to details, a lack of understanding of requirements, a defective design, and unintended and undiscovered performance or quality defects. White wires that are added to a heritage design indicate that the design has been rebaselined and is no longer one-for-one traceable to the heritage design. White wires that are added to create or fix protection circuits will have new and untested failure modes, and are in effect new logic bombs.

The fifth question points to another problem that can be faced when reconfiguring any design, good or bad, and that is a loss of knowledge of the intentions, decisions, and trade-offs originally applied by the designer. The addition of new white wires in an old design represents a change in direction in a design, and may negate features incorporated in the original design.

General considerations for determining risk associated with a modified board

Methods are well established for assuring a successful design built into a PWA using high quality piece parts and PCBs. If modifications are used to correct a failed design the question becomes how do we determine the risk associated with using the modified PWA. The following information that is generally available from standard practices may be used as part of the information base to perform the risk assessment.

1. Analysis
    a. Design Review
    b. Electrical Stress Analysis
    c. FMEA

d Historical Failure / Problem / Anomaly Analysis
e Mechanical Stress Analysis
f. Thermal Analysis
g. Worse Case Analysis

2. Inspection,
   a. Lifted Pads
   b. Oscilloscope Probing*
   c. Point to Point Ring-out
   d. Solder Joints
   e. Staking
   f. Thermal Imaging*
   g. Tight Wires
   h. Wire Placement
3. Results from functional and environmental Testing,
   a. Electrical / Power
   b. EMI
   c. Thermal Vacuum
   d. Vibration

* Could also be located in Testing

Appendix D: Software Heritage Checklist

The following is a checklist that may be used to aid in dispositioning inherited software.

Heritage Analysis			
	Criteria for Evaluation	**Heritage/Re-use Determination**	**Supporting Documentation**
1	**Is there an Acceptance/End-Item data package for the heritage software?**		
1.1	**Planning Baseline**		
1.1.1	Development Plan		
1.1.2	CM Plan		
1.1.3	Test Plan		
1.1.4	Assurance Plan		
1.2	**Requirement Baseline**		
1.2.1	Functional Specifications		
1.2.2	Design Specifications		
1.3	**Code Baseline**		
1.3.1	Unit/Tasks		
1.3.2	Subsystem/Modules		
1.3.3	Flight Image and VDD		
1.4	**V&V Baseline**		
1.4.1	Unit Test Drivers and Test Results		
1.4.2	Integration Test Procedures and Results		
1.4.3	Test Software & Simulators		
1.4.4	Acceptance Test Scenarios, Procedures and Results		
1.4.5	RVTM		
1.4.6	Discrpeancy/Problem Reports		
1.5	**Operations Baseline**		
1.5.1	VDD		
1.5.2	User Manual		
1.5.3	Command and Telemetry Definitions		
2	**Has the intended use of software changed?**		
2.1	Has the operating environment changed (per mission objectives)?		
2.2	Will the allocation of mission requirements to software remain as-is?		
3	**Has the target architecture for software changed?**		
3.1	Processor		
3.2	OS		
3.3	PLDs		
3.4	Memory		
3.5	Avionics Bus		
3.6	Interface Cards		
4	**Can the software requirements be inherited without modifications?**		
4.1	Functional Requirements		
4.2	Design Specifications		
4.3	Interface Requirements/Specifications		
5	**Can the software code be inherited without modifications?**		
5.1	Will the heiritage software image be loaded as-is?		
5.2	Will the heritage source code be compiled as-is?		
5.3	Can existing liens be resolved without changing code?		
6	**Are there sufficient resources for maintenance of the heritage code?**		
6.1	Available staff from the development and test of the heritage project?		
6.2	Access to a high-fidelity maintenance test-bed?		
6.3	Lessons Learned		

Appendix E: FPGA Peer Review information

The following information should be provided from FPGA peer reviews for prior application

Peer review information from the prior application should encompass the following as available for inherited items:

a. Design (place and route) database and any constraint file(s)
b. Synthesis report files
c. Synthesis constraint files
d. Timing analyses for external inputs and outputs, internal domain(s), etc.
e. Static timing analysis results including best and worst case, and least margin/slack for each
f. Disposition of all clock domain crossings
g. Source code (eg VHDL or Verilog), PDF of schematics and/or state machines/tables
h. Requirements, specifications, and verification document(s), and any supporting material relevant to the FPGA
i. Design review documentation, presentations, and action item dispositions
j. Block diagram
k. Simulation code coverage analysis and simulation testbench/script code
l. Source code for 3rd party intellectual property code and/or cores
m. FPGA Design Checklist as per 500-PG-8700-2.7, or equivalent
n. Board(s) schematics containing this FPGA
o. Board netlist(s) (any ASCII format such as PADS, MGC, Allegro)
p. The final peer review report

The following items provide additional useful information to aid in determining risk:

a. System, box, and circuit board requirements, specifications, presentations, and/or verification document(s) relevant to the FPGA and its role in the system, box, and board
b. Board(s) schematics containing this FPGA
c. Board netlist(s) (any ASCII format such as PADS, MGC, Allegro)
d. Board part list (any ASCII or common spreadsheet format)
e. PDF of the board layout, such as an assembly drawing
f. Signal integrity analyses relevant to this FPGA
g. Power integrity analyses relevant to this FPGA

CHANGE HISTORY LOG

Revision	Effective Date	Description of Changes
Baseline	03/28/2016	Initial Release